66793 U.S. PTO
05/21/98

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Check Box, if applicable [ ] Duplicate

Attorney Docket No.	980673	Total Pages	
First Named Inventor or Application Identifier			
Kenji NAGASE			
Express Mail Label No.			

APPLICATION ELEMENTS FOR:

POWER SUPPLY CIRCUIT AND CCD CAMERA USING SAME

ADDRESS TO: Assistant Commissioner for Patents
BOX PATENT APPLICATIONS
Washington, D.C. 20231

1. [XX] Fee Transmittal Form (Incorporated within this form)
(Submit an original and a duplicate for fee processing)

2. [XX] Specification Total Pages [16]

3. [XX] Drawing(s) (35 USC 113) Total Sheets [4]

4. [XX] Oath or Declaration Total Pages [2]

a. [XX] Newly executed (copy)

b. [ ] Copy from prior application (37 CFR 1.63(d)
(for continuation/divisional with Box 17 completed).

i. [ ] Deletion of Inventor(s)
Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation by reference (useable if box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement Verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [XX] Assignment Papers (cover sheet and document(s))

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [XX] Power of Attorney

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10. [ ] English translation Document (if applicable)

11. [ ] Information Disclosure Statement [ ] Copies of IDS Citations

12. [ ] Preliminary Amendment

13. [XX] Return Receipt Postcard (MPEP 503)

14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired.

15. [ ] Claim for Convention Priority [ ] Certified copy of Priority Document(s)

a. Priority of _____ application no. _____ filed on _____ is claimed under 35 USC 119. The certified copies/copy have/has been filed in prior application Serial No. _____.
(For Continuing Applications, if applicable)

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17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

[ ] Continuation [ ] Division [ ] Continuation-in-part (CIP) of prior application no. _____/_____

FEE TRANSMITTAL The filing fee is calculated below	Number Filed	Number Extra	Rate	Basic Fee $790.00
Total Claims	7 - 20		x $22.00	
Independent Claims	4 - 3	1	x $82.00	82.00
Multiple Dependent Claims			$270.00	
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[XX] A check in the amount of $912.00 is enclosed to cover the filing fee of $872.00 and the assignment recordation fee of $40.00.

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18. CORRESPONDENCE ADDRESS

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MRQ/yap

TITLE OF THE INVENTION

Power Supply Circuit and CCD Camera Using Same

BACKGROUND OF THE INVENTION

Field of the invention

This invention relates to a power supply circuit and a CCD camera using the same, and more particularly to a power supply circuit for supplying a positive polarity power voltage and a negative polarity power voltage, particularly, to a camera using a CCD imager or a display unit using an LCD panel, for example.

Description of the prior art

The motion-picture and/or still-picture cameras using, for example, a CCD imager usually require four power voltages of 3.3V, 5V, 15V and −7.5V, and accordingly use a positive/negative-voltage power supply circuit.

In the positive/negative-voltage power supply circuits, there is a necessity that each terminal of the CCD imager be satisfied by an absolute maximum rating of CCD when turning on or off a power switch of the camera. In particular, there may be a case that the above requirement cannot be satisfied due to a long discharge period of time (voltage attenuation time period) for a comparatively high voltage, such as 15V and −7.5V, upon turning off the power switch.

Meanwhile, the discharge time period during turning off the power is determined by a capacitance of a smoothing capacitor and an input impedance on a load (CCD imager) side. Therefore, the discharge time can be optimally set by adjusting a discharging resistance and a capacitance of a smoothing capacitor connected in parallel with the load. That is, the discharge time can be shortened by decreasing the capacitance of the smoothing capacitor and/or reducing the discharge resistance.

However, there is a limitation in decreasing the capacitance of the smoothing capacitor because there arises inconvenience in securing a performance, such as increase of noises, of a power supply circuit. On the other hand, the reduction in discharge resistance results in increase in steadily-consumable current (load current), giving rise to another problem such as lower in efficiency for the power supply circuit.

SUMMARY OF THE INVENTION

Therefore, it is a primary object of this invention to provide a power supply circuit which is capable of shortening the discharge period of time without the necessity of decreasing smoothing-capacitor capacitance or discharge resistance.

It is another object of this invention to provide a power supply circuit which can improve a starting characteristic of a fly-back circuit.

A power supply circuit according to this invention, comprises: a first circuit for generating a positive polarity voltage; a first terminal for outputting the positive polarity voltage from the first circuit; a second circuit for generating a negative polarity voltage; a second terminal for outputting the negative polarity voltage from the second circuit; and a short circuit for short-circuiting substantially between the first terminal and the second terminal in response to a power-off signal.

For example, when the power switch of a camera is turned off, a micro-computer of the camera outputs a power-off signal. In response to this power-off signal, a PWM switching controller, for example, is disabled. At the same time, the first terminal and second terminal are short-circuited substantially therebetween through a short-circuit.

Where the short circuit includes a series circuit of a switching element and a current-limiting element, the switching element is turned on by a power-off signal. Accordingly, a current flows through the current-limiting element due to the residual

charges on the respective smoothing capacitors connected to the first and second terminals. The current is dissipated as thermal energy by the current-limiting element. Therefore, the residual electric charges are promptly discharged to thereby shorten the discharge time for the positive-polarity voltage and the negative-polarity voltage.

Even where the short-circuit does not contain a current-limiting element, the above-stated current due to the residual charges is dissipated by an internal resistance (on resistance) of the switching element. Therefore, the residual charges are promptly discharged in a similar manner, shortening the discharge time for the positive-polarity voltage and the negative-polarity voltage.

The power supply circuit is employed in a CCD camera so that respective positive polarity voltage and negative polarity voltage are supplied to a CCD imager thereof.

According to this invention, the discharge time during current-off can be shortened by merely connecting a short-circuit between the first terminal and the second terminal, without the necessity of reducing smoothing capacitor capacitance or discharge resistance.

According to one aspect of this invention, the first circuit includes a chopper circuit for generating a low first positive voltage, and a fly-back circuit for receiving the first positive voltage from the chopper circuit to generate a high second positive voltage, wherein the power supply circuit further comprises: first and second output terminals for respectively outputting the first positive voltage and the second positive voltage; and a diode connected between the first and second output terminals in a forward direction of from the first positive voltage output terminal to the second positive voltage output terminal.

In the above-stated power supply circuit, however, the second circuit for generating the negative polarity voltage may be omitted. In such a case, a power supply

circuit, comprising: a chopper circuit for generating a low first voltage; a fly-back circuit for receiving the first voltage from the chopper circuit to generate a high second voltage; first and second terminals for respectively outputting the first and second voltages; and a diode connected between the first terminal and the second terminal in a forward direction of from the first terminal to the second terminal.

In this aspect, when a power switch of the camera for example is turned on, a power-on signal is outputted from a micro-computer of the camera. A PWM-switching controller, for example, is enabled in response to this power-on signal. The chopper circuit accordingly generates a first voltage. This first voltage is outputted to the first terminal, which in turns outputted from the first terminal to the second terminal through the diode. Accordingly, when the chopper circuit is started, the second terminal immediately has a voltage outputted thereto. Then, if fly-back circuit is started and the second voltage exceeds over the first voltage, a reverse bias is applied to the diode and turns off the same diode.

In this manner, a first voltage from the chopper circuit is outputted at the first terminal, and simultaneous therewith a voltage output is given at the second terminal. Therefore, the starting characteristic is improved, and the absolute maximum rating of the CCD imager can be satisfied.

The power supply circuit is employed in a CCD camera so that respective positive polarity voltage and negative polarity voltage are supplied to a CCD imager thereof.

The above described objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram showing one embodiment of this invention;

Figure 2 is a graph showing a discharge time in the Figure 1 embodiment, wherein the horizontal axis denotes time while the vertical axis voltage;

Figure 3 is a graph showing discharge time in a prior art lacking a short-circuit of the Figure 1 embodiment, wherein the horizontal axis denotes time while the vertical axis voltage;

Figure 4 is a circuit diagram showing another embodiment of this invention;

Figure 5 is a graph showing a starting characteristic in the Figure 4 embodiment, wherein time is represented by a horizontal axis and voltage by a vertical axis; and

Figure 6 is a graph showing a starting characteristic of a prior art lacking a diode of the Figure 4 embodiment, wherein time is represented by a horizontal axis and voltage by a vertical axis.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to Figure 1, a positive/negative-voltage power supply circuit 10, in this embodiment, is utilized as a power supply circuit of a camera 12. It should be noted beforehand that the positive/negative-voltage power supply circuit of this invention can be also utilized as a power supply for a display unit using an LCD panel etc., besides for a camera.

The camera 12 includes a CCD imager 14 and a timing generator 16 for supplying various drive voltages to the CCD imager 14. These CCD imager 14 and the timing generator 16, in this embodiment, are supplied with two power voltages of 15V and −7.5V from the power supply circuit 10. The camera 12 further includes a micro-computer 18 to control the overall operation of the camera 12. This micro-computer 18 receives an operational signal from the power switch 20. The micro-computer 18 operates on a

power voltage of, for example, 5V or 3.3V. When the power switch 20 is turned on, the micro-computer 18 outputs a power-on signal. If the power switch 20 is turned off, the micro-computer 18 outputs a power-off signal. The power-on signal and the power-off signal are illustrated as power-supply control signals in Figure 1.

The power supply circuit 10 includes a switching controller 22. This switching controller 22 is supplied with the above-stated power supply control signal. Accordingly, the switching controller 22 is enabled by the power-on signal, and disabled by the power-off signal. The switching controller 22 receives a power voltage VB from, for example, a battery (not shown). The switching controller 22, when enabled, outputs a switching signal according, for example, to a PWM method to a base of a pnp transistor Q1. The emitter-collector of the transistor Q1 is connected between a power voltage from a battery and one terminal of a primary winding of a transformer T. The other terminal of the primary winding of the transformer T is grounded.

Two circuits 24 and 26 are formed on a side of a secondary winding of the transistor T. The circuit 24 functions as a first circuit to generate a positive-polarity voltage, e.g. 15V. The circuit 26 serves as a second circuit to create a negative polarity voltage, e.g. -7.5V. The voltage 15V generated by the first circuit 24 is outputted through a first terminal 24a to the CCD imager 14 of the camera 12 and the timing generator 16 for supplying various drive voltages to the CCD imager 14. The camera 12 further includes a clamp circuit 17. The voltage -7.5V generated by the second circuit 26 is outputted through a second terminal 26a to the CCD imager 14 and the timing generator 16.

The first circuit 24 is so-called a fly-back circuit, and includes a rectifying diode D1 connected to the first terminal of the secondary winding of the transformer T, a smoothing capacitor C11 for receiving a direct-current voltage from the diode D1, and a filter formed by a choke coil L1 and capacitor C12 connected to the smoothing capacitor

C11. The second circuit 26 is also a fly-back circuit, and includes a rectifying diode D2 being connected to a second terminal of the secondary winding of the transformer T, a smoothing capacitor C21, and a filter formed by a choke coil L2 and a capacitor C22.

In this embodiment, between the first terminal 24a and the second terminal 26a is connected a short-circuit 28 which includes an FET Q2 functioning as a switching element and a resistance R1 connected in series to the FET Q2. That is, the FET Q2 has a source connected to the first terminal 24a, and a drain connected to one end of the resistance R1. The other end of the resistance R1 is connected to the second terminal 26a. A pull-up resistance R2 is connected between the source and the gate of the FET Q2.

The gate of the FETQ2 forming the short-circuit 28 is connected to a collector of an npn transistor Q3. The transistor Q3 has an emitter grounded, and a base connected with biasing resistances R3 and R4. The resistance R4 is connected with a speed-up capacitor C1 in parallel therewith. The base of the transistor Q3, therefore, is connected to a collector of an npn transistor Q4 through a parallel circuit of the resistance R4 and the capacitor C1. The collector of the transistor Q4 is connected to a power voltage VB of a battery (not shown) through a collector resistance R5. The transistor Q4 at a base receives the above-stated power supply control signal outputted from the micro-computer 18 of the camera 12.

In response to turning-on of the power supply switch 20, the micro-computer 18 outputs a power-on signal, e.g. 5V. In response thereto, the switching controller 22 is enabled to output 15V to the first terminal 24a and -7.5V to the second terminal 26a, according to a well-known PWM method. On the other hand, since the power-on signal is applied to the base of the transistor Q4, this transistor Q4 is turned on. The transistor Q3 at its base becomes 0V. The transistor Q3 is turned off. At this time, the gate of the FETQ2 is pulled-up to 15V by a resistance R2, and accordingly the FET Q2 is off.

Accordingly, the short-circuit 28 is not in operation, and the first circuit 24 and the second circuit 26 continue their normal operations.

In response to turning-off of the power supply switch 20, the micro-computer 18 outputs a power-off signal, e.g. 0V. In response thereto, the switching controller 22 is disabled to stop the operation of the first circuit 24 and the second circuit 26. Accordingly, both the voltage 15V at the first terminal 24a and the voltage −7.5V at the second terminal 26a are shut off. However, electric charges are built up on the smoothing capacitors C11 and C21 and the filter capacitor C12 and C22, and the voltages 15V and −7.5V will not immediately drops to 0V.

On the other hand, the power-off signal is applied to the base of the transistor Q4, and turning off the transistor Q4. Accordingly, the transistor Q3 is applied at the base by a biasing voltage determined by the voltage VB and the resistances R5, R4 and R3. Therefore, the transistor Q3 is turned on so that the FET Q2 has a gate voltage of 0V. Thus the FET Q2 is turned on. This causes the short-circuit 28 to operate so that the first terminal 24a and the second terminal 26a are short-circuited therebetween through the resistance R1. Accordingly, the positive electric charges stored on the smoothing capacitor C11 and the filter capacitor C12 and the negative electric charges on the smoothing capacitor C21 and the filter capacitor C22 causes a current flowing through the resistance R1. At this time, the amount of the current is restricted by the resistance R1 so as not to cause an excessively high rush current flowing through the FET Q2. That is, the resistance R1 serves as a current-limiting resistance.

If a current flows through the current-limiting resistance R1 due to operation of the short-circuit 28, the current-limiting resistance R1 is heated up by this current. In other words, the residual charges on the capacitors C11, C12, C21 and C22 are dissipated as thermal energy by the resistance R1. Therefore, the residual charges decreases to 0 in a

short time.

In the Figure 1 embodiment, the discharge time of period for the voltage 15V, -7.5V is shortened to, for example, around 7.5 milli-seconds in this manner as shown in Figure 2. Incidentally, in the prior art lacking a short-circuit 28 and its peripheral circuits with respect to the Figure 1 embodiment, the discharge time for 15V is approximately 200 milli-seconds, and the discharge time for -7.5V is about 20 seconds that is further longer. It is therefore understood from the Figure 1 embodiment that the discharge time can be greatly shortened without changing the smoothing capacitor or discharge resistance (not shown).

Where the first circuit 24 and the second circuit 26 respectively of 15V and -7.5V are independently provided in the Figure 1 embodiment, it is possible to separately adjust the discharge time so as to satisfy the rating stated before. However, even if the first circuit 24 and the second circuit 26 are provided with individual transformers, it is impossible to solve the problem that the discharge time for -7.5V is excessively long similarly to the prior art so long as the switching controller 22 is commonly provided thereto.

Incidentally, it is needless to say that the polarity of the FET Q2 in the short-circuit 28 or other transistors Q3 - Q4, etc. or the polarity of the power supply control signal can arbitrary selectively set.

The short-circuit 28 may be formed only by switching elements such as FETs. In such a case, since there is no current-limiting resistance, the residual charges are discharged (consumed as thermal energy) through the on-resistance of the switching element.

Also, where no current-limiting resistance is provided in the short-circuit 28, it is expected that the rush current due to the residual charges increases. In such a case, a

greater current rating of a switch element is preferably employed.

The switching element may use a bipolar transistor, GTO, etc., besides the FET as in the embodiment.

A motion and/or still picture camera using, for example, a CCD imager, as in the Fig. 1 embodiment, usually requires a lower power voltage, such as 3.3V or 5V, and a higher power voltage, such as 15V. In the power supply circuit for a CCD camera, therefore, a lower voltage circuit is usually realized by means of a chopper method while a higher voltage circuit by a fly-back method using a transformer.

Accordingly, the power supply, at a start, is in such an output characteristic that is prolonged in start-up time for the higher voltage circuit, as compared to that of the lower voltage circuit. There may be a case that an absolute maximum rating is not satisfied for the CCD imager.

There is a limitation of transformer characteristic to shorten a start-up time for the higher voltage circuit. Due to this, it could be considered that the start-up time of the lower voltage circuit be increased to harmonize with the start-up time for the higher voltage circuit. However, where the high voltage circuit is formed in such a configuration as to receive an output from the lower voltage circuit so as to generate a higher voltage, if the start-up time be increased for the lower voltage circuit, the start-up time for the higher voltage circuit is also increased together therewith. That is, it is impossible to improve the above-stated starting characteristic by merely setting soft start.

In order to solve such a problem, a Fig. 4 embodiment is illustrated. The Fig. 4 embodiment is a modification to the Fig. 1 embodiment, wherein the second circuit 26 of the Fig. 1 embodiment, i.e. a portion related to the negative-polarity voltage, is omitted.

Referring to Figure 4, a power supply circuit 10, in this embodiment, is utilized as a power supply circuit of a camera 12. This camera 12 includes a CCD imager 14, a

timing generator 16 for supplying various drive voltages to the CCD imager 14, and a clamping circuit 17. The CCD imager 14 and the timing generator 16, in this embodiment are each supplied with two power voltages of 15V and 5V from the power supply circuit 10. The clamping circuit 17 is supplied with 15V. The camera 12 further includes a micro-computer 18 to control the overall operation of the camera 12. This micro-computer 18 receives operational signals from the power switch 20. The micro-computer 18 operates on a power voltage of, e.g. 3.3V, not shown. When the power switch 20 is turned on, a power-on signal is outputted from the micro-computer 18, while if the power switch 20 is turned off, a power-off signal is outputted from the micro-computer 18. The power-on signal and the power-off signal are illustrated as power supply control signals in Figure 4.

The power supply circuit 10 includes a switching controller 22 so that this switching controller 22 is supplied with the above-stated power supply control signals. Accordingly, the switching controller 22 is enabled by the power-on signal, and disabled by the power-off signal. The switching controller 22 receives a power supply voltage VB, for example, from a battery (not shown) so that it outputs a switching signal to a base of a pnp transistor Q5 according to, for example, a PWM method. The transistor Q5, constituting a chopper circuit 30, has an emitter to receive the battery power voltage VB and a collector connecting with a fly-wheel diode D3. The chopper circuit 30 further includes a chopper coil L3 to receive a collector voltage of the transistor Q5, a smoothing capacitor C3, and a choke coil L4 and a capacitor C4 both connected to the smoothing capacitor C3. The chopper circuit 30 is a circuit to generate a lower power voltage, e.g. 5V. The lower power voltage generated by this chopper circuit 30 is outputted through the first terminal 24b, and supplied to the CCD imager 14 and the timing generator 16 of the CCD camera 12.

On the other hand, the output of the smoothing capacitor C3 of the chopper circuit 30 is supplied as an input voltage to the fly-back circuit 24 for generating a high power voltage. The fly-back circuit 24 includes a pnp transistor Q1, and an emitter of which receives a direct current supplied from the smoothing capacitor C3. A collector of the transistor Q1 is connected to one terminal of a primary winding of a transformer T. The primary winding of the transformer T has another terminal being grounded.

The fly-back circuit 24 includes a rectifying diode D1 connected to one terminal of a secondary winding of the transformer T, a smoothing capacitor C11 for receiving a d.c. voltage from the diode D1, and a filter formed by a choke coil L1 connected to the smoothing capacitor C11 and a capacitor C12. The fly-back circuit 24 generates a higher power voltage, e.g. 15V, so that this 15V is outputted through the second terminal 24a to the CCD imager 14 of the CCD camera 12, the timing generator 16 and the clamping circuit 17 of the CCD camera 12.

In this embodiment, a diode D4 is connected between the first terminal 24b and the second terminal 24a in a forward direction of from the first terminal 24b to the second terminal 24a.

Responsive to turning-on of the power supply switch 20, the micro-computer 18 outputs a power-on signal, e.g. 5V. In response thereto, the switching controller 22 is enabled to start the chopper circuit 30 according to a well-known PWN method. Consequently, the first terminal 24b of the chopper circuit 30 has a power voltage according to starting characteristic of the chopper circuit 30, as shown by a line A in Figure 5. On the other hand, the fly-back circuit 24 has a long start-up time so that the second terminal 24a at this time has no power voltage output as shown by a line B in Figure 6. However, in the Figure 4 embodiment the first terminal 24b and the second terminal 24a has the diode D4 connected therebetween so that the voltage generated by

the chopper circuit 30 is also supplied to the second terminal 24a through the diode D4. Accordingly, the second terminal 24a has an output voltage outputted simultaneously with the start of the chopper circuit 30, as shown by a line C in Figure 5. That is, if there is a difference between the timing of output of a power voltage through the first terminal 24b and the timing of output of a power voltage through the second terminal 24a as shown by the line B in Figure 6, it is impossible to fulfill the absolute maximum rating required by the CCD imager 14. However, if there is an approach between the timing of output through the first terminal 24b and the timing of output through the second terminal as in this embodiment, the above-stated absolute maximum rating can be satisfied.

Thereafter, when the fly-back circuit 24 is started and the voltage generated by the fly-back circuit 24 exceeds the voltage (5V) at the first terminal 24b, the diode D4 is reverse biased. Accordingly, no electric current flows from the second terminal 24a to the first terminal 24b. Therefore, both the two circuits 30 and 24 continue their normal operations.

Incidentally, in the Figure 4 embodiment, the first terminal 24b and the second terminal 24a were connected through the diode. However, this diode may be substituted by a transistor. However, where a transistor is used, an especial circuit is required to control the turning-on/off of the transistor. Therefore, it is preferred to use the diode for simplification.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A power supply circuit, comprising:

a first circuit for generating a positive polarity voltage;

a first terminal for outputting the positive polarity voltage from said first circuit;

a second circuit for generating a negative polarity voltage;

a second terminal for outputting the negative polarity voltage from said second circuit; and

a short circuit for short-circuiting substantially between said first terminal and said second terminal in response to a power-off signal.

2. A power supply circuit according to claim 1, wherein said short-circuit includes a series circuit having a switching element and a current-limiting element connected between said first terminal and said second terminal.

3. A power supply circuit according to claim 1, wherein said short circuit includes a switching element connected between said first terminal and said second terminal.

4. A power supply circuit according to claim 1, wherein said first circuit includes a chopper circuit for generating a low first positive voltage, and a fly-back circuit for receiving the first positive voltage from the chopper circuit to generate a high second positive voltage, and further comprising:

first and second output terminals for respectively outputting the first positive voltage and the second positive voltage; and

a diode connected between said first and second output terminals in a forward direction of from said first positive voltage output terminal to said second positive voltage output terminal.

5. A power supply circuit, comprising:

a chopper circuit for generating a low first voltage;

a fly-back circuit for receiving the first voltage from said chopper circuit to generate a high second voltage;

first and second terminals for respectively outputting the first and second voltages; and

a diode connected between said first terminal and said second terminal in a forward direction of from said first terminal to said second terminal.

6. A camera, comprising:

a first circuit for generating a positive polarity voltage;

a first terminal for outputting the positive polarity voltage from said first circuit;

a second circuit for generating a negative polarity voltage;

a second terminal for outputting the negative polarity voltage from said second circuit;

a short circuit for short-circuiting substantially between said first terminal and said second terminal in response to a power-off signal; and

a CCD imager for receiving the positive polarity voltage and negative polarity voltage through said first terminal and said second terminal.

7. A camera, comprising:

a chopper circuit for generating a low first voltage;

a fly-back circuit for receiving the first voltage from said chopper circuit to generate a high second voltage;

first and second terminals for respectively outputting the first and second voltages;

a diode connected between said first terminal and said second terminal in a forward direction of from said first terminal to said second terminal; and

a CCD imager for receiving the positive polarity voltage and negative polarity voltage through said first terminal and said second terminal.

ABSTRACT OF THE DISCLOSURE

A power circuit includes a switching controller. The switching controller outputs a switching signal to a base of a transistor, according to a PWM method. The output of the transistor is supplied to a primary winding of the transformer. A first circuit and a second circuit are formed on a secondary winding side of the transformer. The first and second circuits generate, respectively, a voltage, e.g. of 15V, and a voltage, e.g., of -7.5V. 15V is outputted through a first terminal, while -7.5V is through a second terminal. The respective voltages are supplied to a CCD imager and a timing generator of a camera. A short circuit, including an FET and a resistance connected in series to the FET, is connected between the first terminal and the second terminal.

FIG. 1

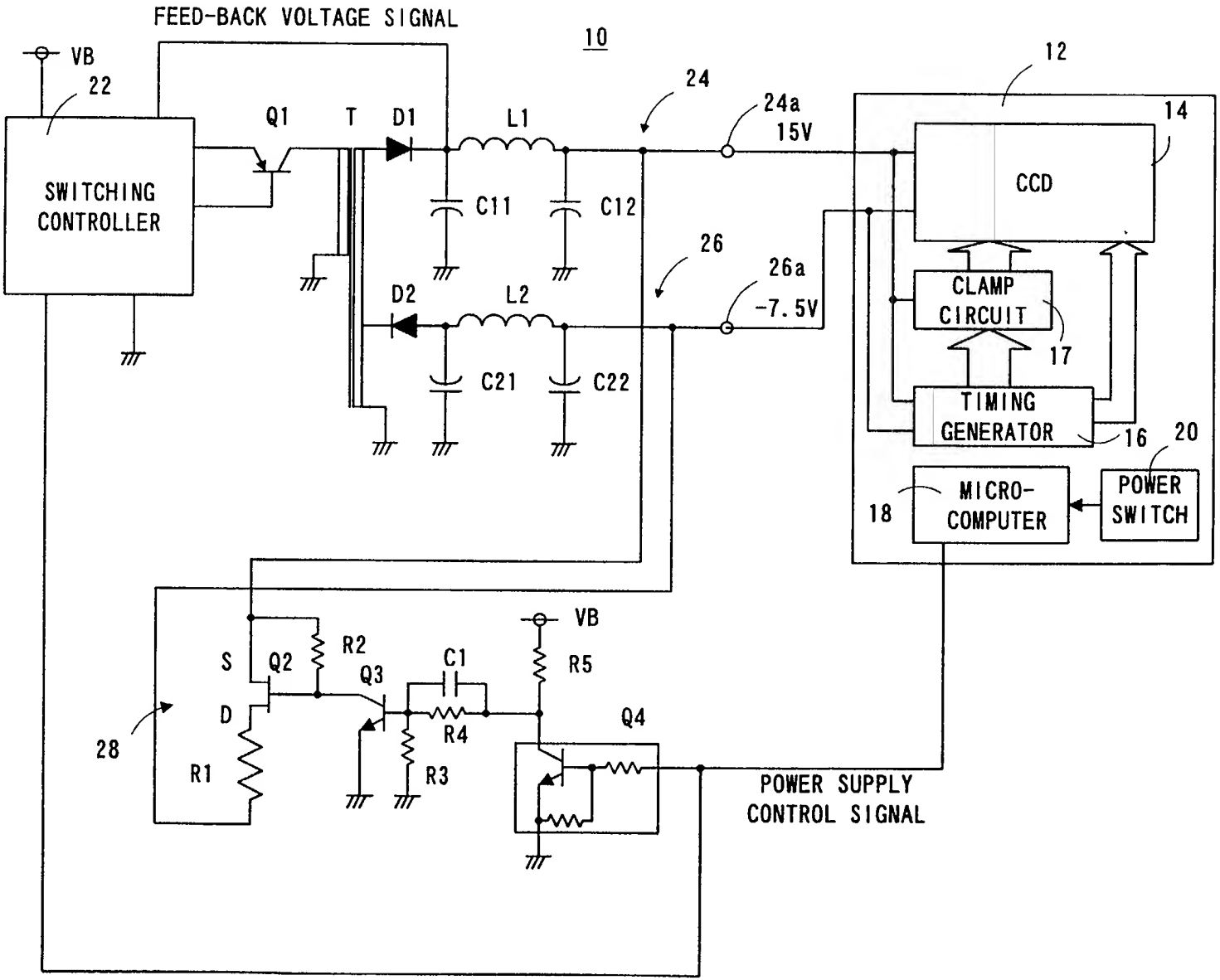

FEED-BACK VOLTAGE SIGNAL
10
VB
22
SWITCHING CONTROLLER
Q1
T
D1
L1
24
24a
15V
12
14
CCD
C11
C12
26
26a
-7.5V
D2
L2
C21
C22
CLAMP CIRCUIT
17
TIMING GENERATOR
16
20
MICRO-COMPUTER
18
POWER SWITCH
VB
S
Q2
R2
Q3
C1
R5
D
R4
Q4
28
R1
R3
POWER SUPPLY CONTROL SIGNAL

FIG. 2

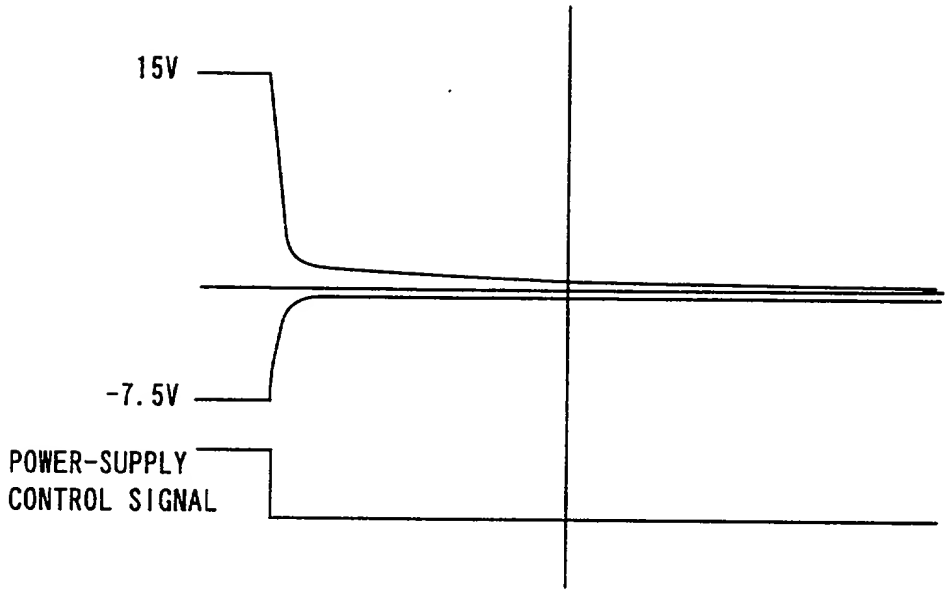

15V
-7.5V
POWER-SUPPLY
CONTROL SIGNAL

FIG. 3

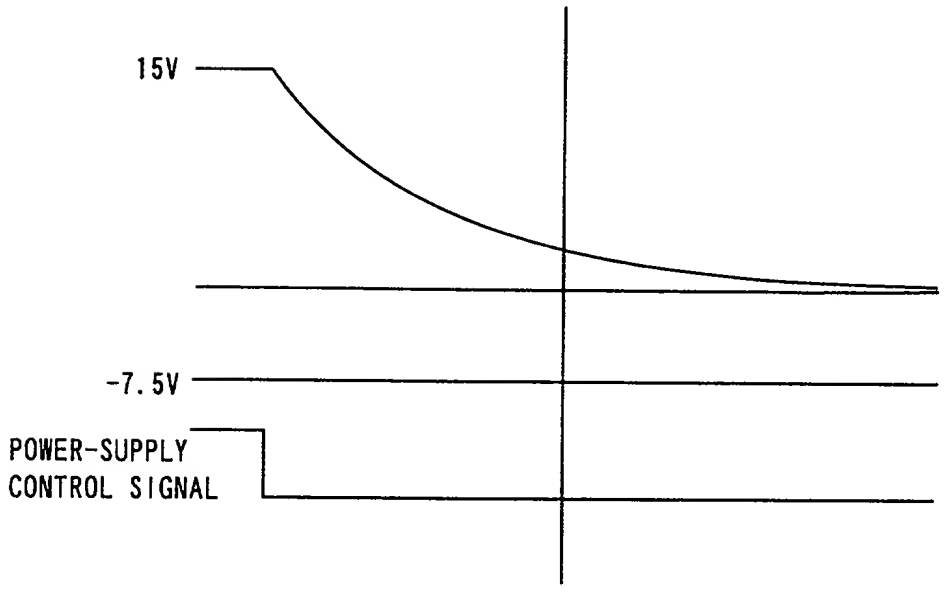

15V
-7.5V
POWER-SUPPLY
CONTROL SIGNAL

FIG. 4

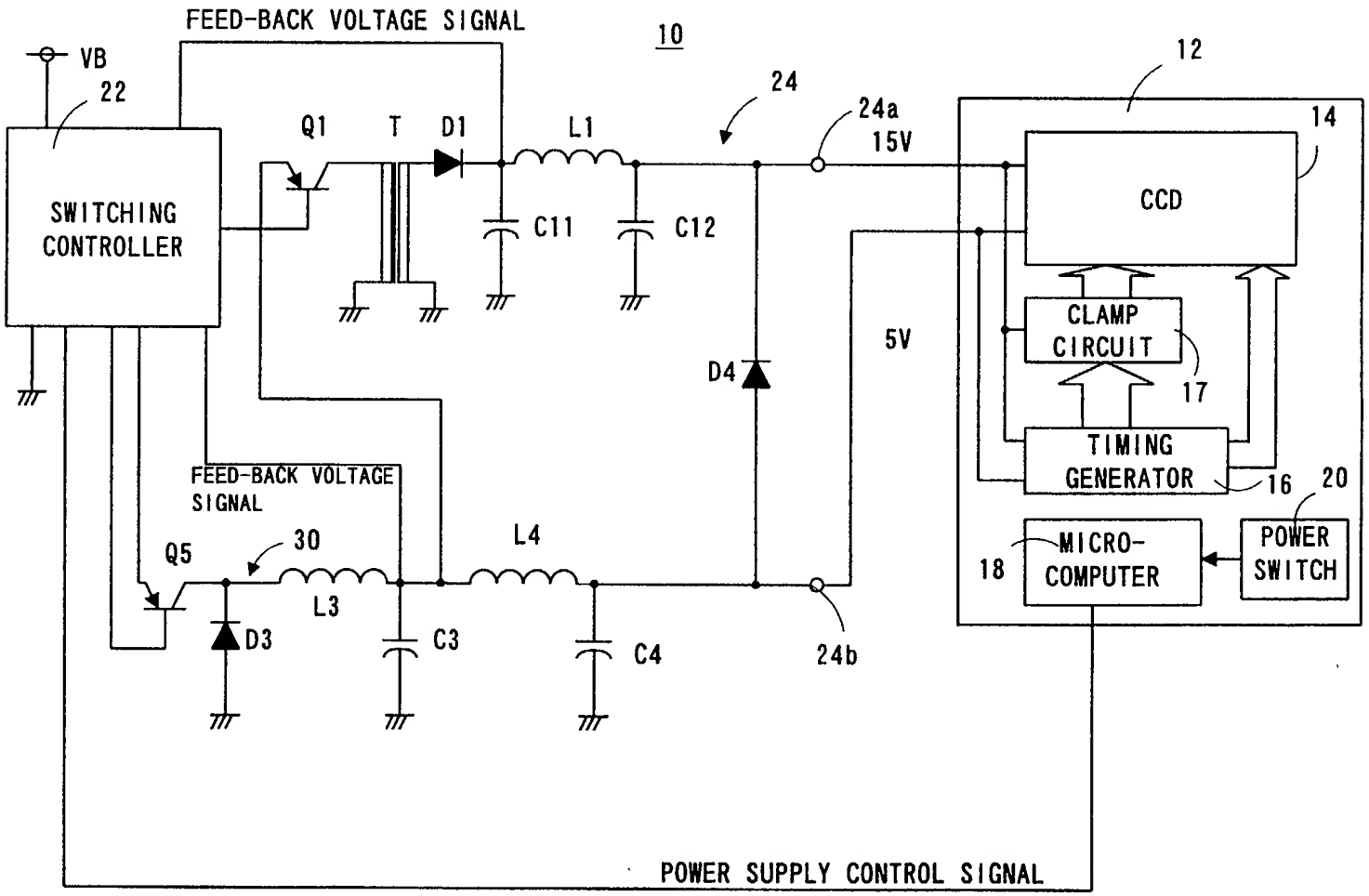


FIG. 5

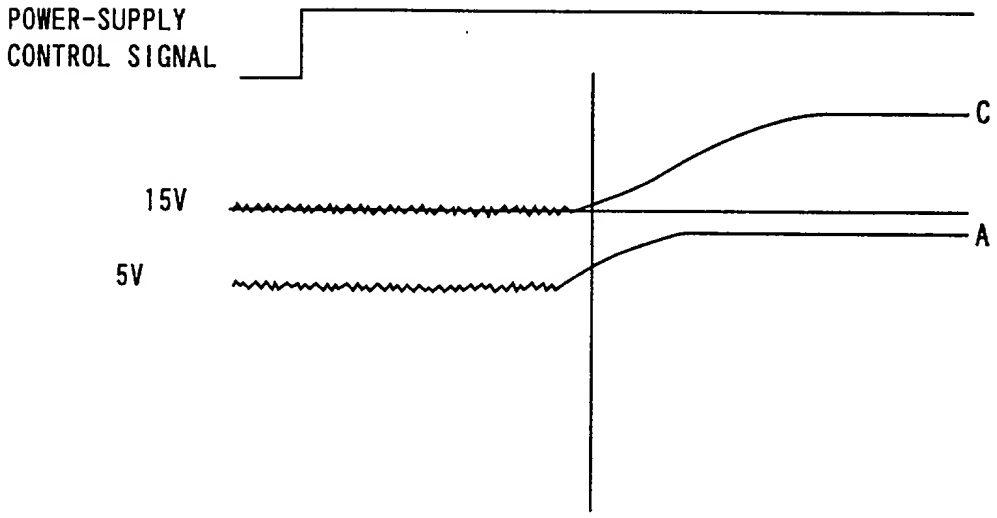
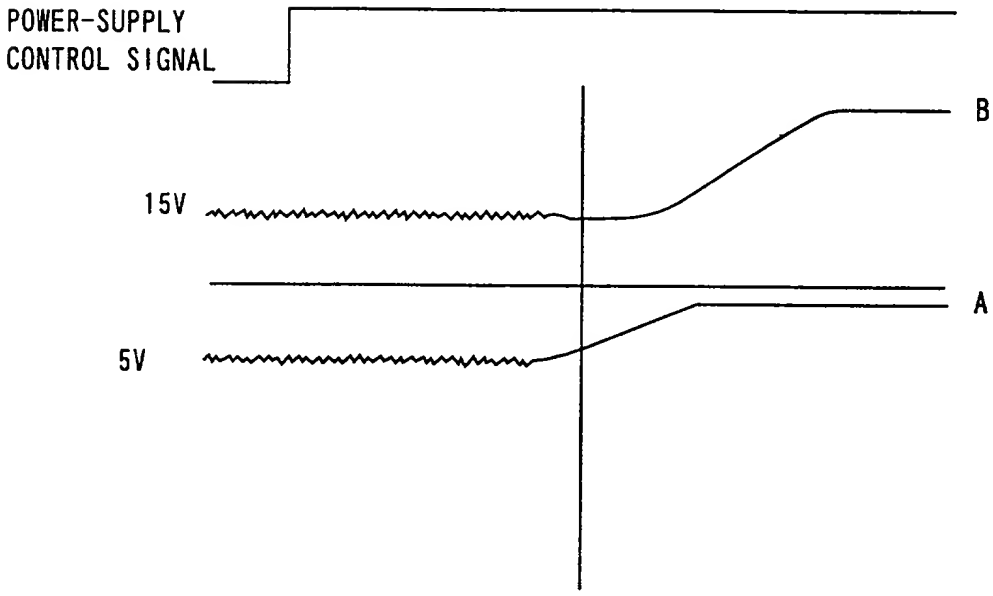

POWER-SUPPLY
CONTROL SIGNAL
C
15V
A
5V

FIG. 6


POWER-SUPPLY
CONTROL SIGNAL
B
15V
A
5V

A, W, H, McL & N Docket No._____ ARMSTRONG, WESTERMAN, HATTORI, MCLELAND & NAUGHTO

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **entitled** (Insert Title) POWER SUPPLY CIRCUIT AND CCD CAMERA USING SAME

the specification of which is attached hereto unless the following is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a) - (d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(List prior foreign applications. See note A on back of this page)	(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
	Pat. Appln. No. 9-131786	Japan	22/5/1997	☒ Yes ☐ No
	No. 9-131787	Japan	22/5/1997	☒ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No

(See note B on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of the application:

(List Prior U.S. Applications)	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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ereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief e believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made e punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements ay jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor (given name, family name) Kenji NAGASE

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ventor's Signature Date

sidence Citizenship

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ll name of fourth inventor (given name, family name)

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ll name of eighth inventor (given name, family name)

ventor's Signature Date

sidence Citizenship

st Office Address